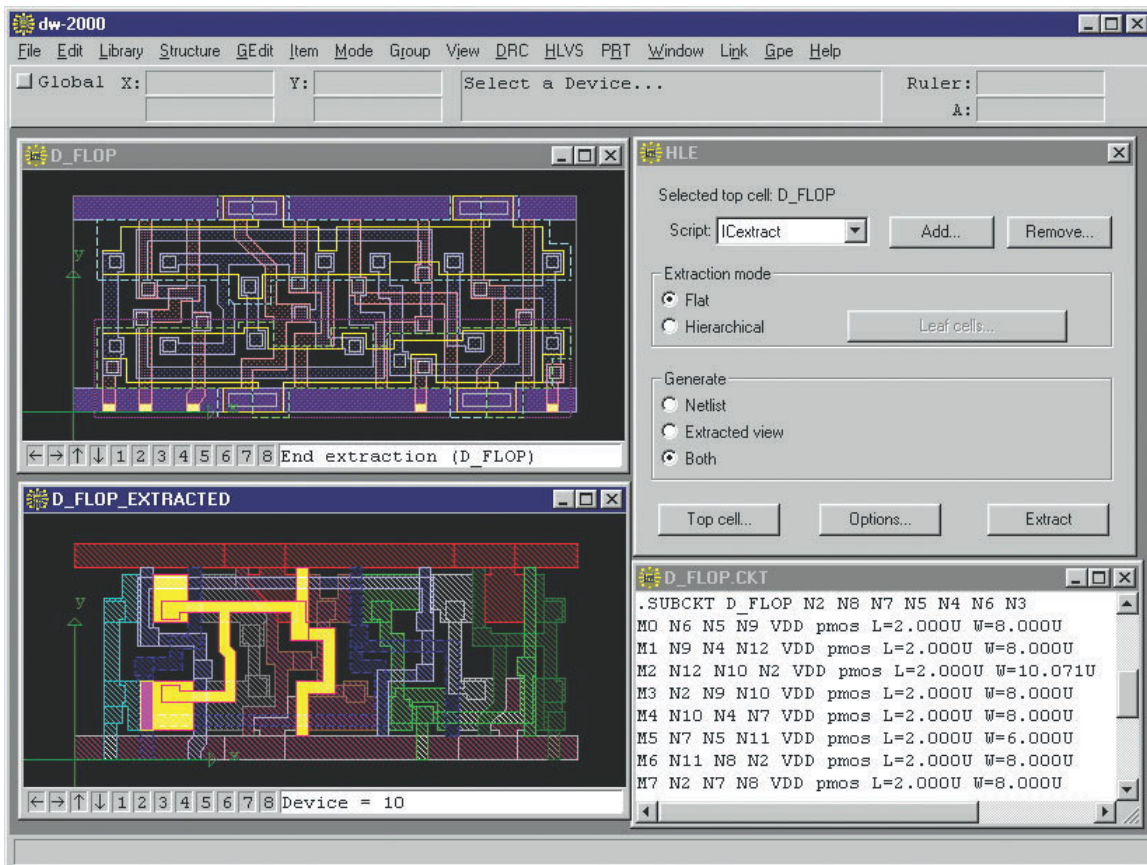# dw-2000™ HLVS

dw-2000 HLVS is the gateway to advanced features such as electrical layout extraction and network comparison. As is true with all dw-2000 modules, HLE and LVS are well-integrated with the dw-2000 programming environment (GPE) and easily customized to address a wide variety of problems. With these modules, you can easily implement extraction rules for any technology or application.

Hierarchical Layout Extraction

HLE is an electrical extractor that translates the physical geometric organization of a circuit layout into an electrical network (or netlist). Based on user-defined relationship information, it proceeds to detect electrical components from the geometrical relationships of the layout and then generates a netlist in HSPICE format either with or without parasitic.

Flat or Hierarchical Extraction

HLE allows you to choose between hierarchical or flat extraction. In the case of a hierarchical extraction, you can select which nested structures to instantiate as "leaf cells" in the netlist. This powerful feature allows the layout hierarchy to be different than the reference netlist hierarchy, thereby freeing you from having to apply the same hierarchy to your layouts.

HLVS

dw-2000™ HLVS

Locating Nets and Devices Easily

HLE also includes a network navigator that allows you to query information about a particular active element or simply highlight a particular net. In the latter case, all the geometries (or portions thereof) constituting this net are highlighted. Combined with the LVS report, it is an easy way to locate and correct electrical problems.

Writing HLE Scripts

HLE provides a rich collection of commands that can be called in GPE scripts. Combined with all the other commands accessible through GPE you can create detailed extraction scripts for different types of technologies.

Layout Versus Schematic

LVS is a network comparator used to compare an electrical network extracted (using HLE) from a physical layout to a reference electrical network in order to detect a mismatch and therefore a physical layout error.

Allowing Acceptable Differences

Due to certain process rules, it is sometimes impossible to re-create certain devices perfectly. Instead of modifying the original reference netlist, you can specify options and tolerance values in order to allow for acceptable differences between the two netlists.

Pin Swapping

By using the options or a mapping file, you can specify that certain device pins are interchangeable, for example, the two inputs of a "NAND".

HLE *Highlights*

- HLE commands are GPE-scriptable; hence usable in users' programs

- HLE Option to generate Hierarchical or Flat netlist (HSPICE format)

- Parasitics extraction

- Electrical view representation and navigation

- Easy-to-use graphical user interface (GUI)

LVS *Highlights*

- LVS netlist support of HSPICE, EDIF and VERILOG formats

- Name-binding option for matching non-symmetrical cell representations

- Matching tolerance and permutability control

- Ability to merge parallel and serial devices

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